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TITLE: PHOTORESIST
COMPOSITION

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ABSTRACT:

PURPOSE: To provide a novel photoresist composition used for lithography by the use of ultraviolet ray and particularly to provide the photoresist composition capable of lithography of submicron by far ultraviolet ray (DUV) and free from the distortion of an image even at the time of high temp. treating such as plasma etching executed at above 170°C, sputtering or ion implantation.

CONSTITUTION: The photoresist composition consists of an alkali soluble polymer and a bisazide sensitizer of sufficient quantity to cross-link the alkali soluble polymer by irradiation with ultraviolet and the alkali soluble polymer is composed of indene and maleimide or a polymerizing component of

naphtha oil, which is composed mainly of indene and contains (A) 70-99wt.% indene, (B) 0.5-29.5wt.% styrene and (C) 0.5-29.5wt.% one kind or two or more kind selected from a group composed of α -methyl styrene, methyl styrene, dimethyl styrene, trimethyl styrene, methyl indene, coumarone and dicyclopentadiene, and maleimide.

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DISCLOSURE TITLE: Self-Aligned Pocket
Implantation Technology for Forming a
Halo Type Device using Selective
Tungsten Deposition.

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DISCLOSURE TEXT:

This document contains drawings, formulas,
and/or symbols that
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- A technique to manufacture a localized self-aligned pocket implantation to form a "halo" type MOSFET device is presented. The localized pocket is formed by implantation using the gate electrode of the MOSFET device and a selectively deposited tungsten films as self-aligned masks. This technique provides high punch-through resistance, decreased V_t roll-off, high current capability device while maintaining low source/ drain junction capacitance and good device reliability compared to present techniques of forming a halo type FET device.
- To decrease the short-channel effects in MOSFETs, the substrate doping has to be raised. However, this increases the source and drain junction capacitance and lowers the device current drive. This high capacitance and lower current result

in reduced circuit speed, cancelling partially the beneficial effects of channel shortening. By increasing the substrate doping in the source and drain regions near the channel while keeping it as low as possible in the channel region, we can improve the short-channel behavior of the MOSFET device without significantly affecting its drain junction capacitance and current drive capability.

- One solution to this problem is described in 1ù. A standard CMOS process with SALICIDED source/drain junctions is utilized.

The nitride spacer formed before source drain salicidation is removed and Boron is implanted (in n-channel devices) obliquely through this hole. The TiSi_2 prevents the doping from extending around the junction, while the angle implant allows the doping to reach below the channel. However, this process, although it achieves

the desirable channel doping below the channel, forbids to remove or anneal the damage to the gate oxide due to the oblique implantation, because:

1. The quality of the TiSi sub 2 layer is adversely affected by an anneal at high temperature ($>800^{\circ}\text{C}$) which is required to repair damage caused to the gate oxide during the "halo" implantation.

- 2.

The thermal cycle required to anneal the gate damage described in point 1 will result in deeper source drain junctions as well as a deeper halo region. This will result in poor short channel device characteristics.

3. TiSi sub 2 cannot withstand an HF dip which might be required before the anneal in point 1. This is because TiSi sub 2 is etched far faster than the oxide.

This paper describes a new technique to solve these problems.

- Proposed is the use of a standard CMOS process with or without silicide. The halo implant is formed prior to source/drain implants. The poly-gate and a selectively deposited tungsten film (or any other implant blocking film that can be selectively deposited over the source/drain junctions) are utilized as a self-aligned masks to implant the "halo" localized implants. The detailed process is described below.

- The proposed process flow using selective tungsten deposition is as follows. Although the steps describe the fabrication of n-channel device, the technique can also be used for a p-channel device using the appropriate implant species.

1. Implant channel for the threshold voltage adjustment, grow the gate oxide, deposit 200nm of polysilicon, pattern, clean.
2. Poly oxidation (10nm) to remove RIE

damage and to prevent
implant damage.

3. Form a Si sub 3 N sub 4 spacer (100nm)
4. Selectively deposit 30nm of tungsten 2ù
over the polysilicon
gate and the source-drain regions (Fig. 1).
5. Selectively etch the Si sub 3 N sub 4
spacer (Fig. 2), leaving
the 10nm oxide as a protection for the gate
area
6. Angle implant Boron, to manufacture the
"halo" pocket implant for
improved short-channel characteristics (Fig.
3).
7.
Selectively wet etch tungsten
8. HF dip and anneal to remove the gate
oxide damage
9. Implant the source drain junctions and
drive-in.
10. Resume standard CMOS processing.
- A variation of this is to use selectively
deposited oxide.

In that case, the process flow is slightly
modified. Instead of
selectively depositing tungsten, oxide 3ù was
selectively

deposited. The selective tungsten etch is replaced by a selective RIE of oxide. The etch has to be selective to silicon, otherwise a nitride layer has to be used as an etch stop.

- Independently of which material is used, the masking layer thickness cannot be too big, due to the shadowing during the angle implant.
- This method of making pocket implants can be used in any CMOS technology, for both n- and p-channel devices (buried channel and surface channel).

References

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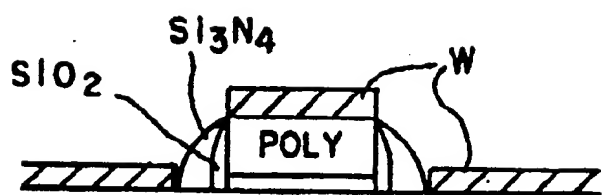


FIG. 1

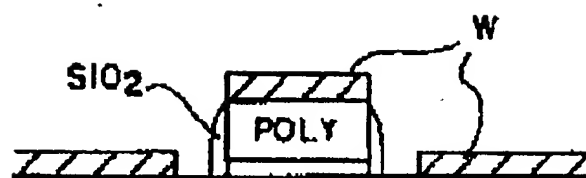


FIG. 2

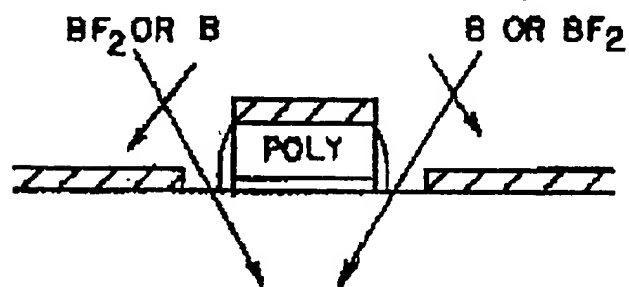


FIG. 3